**Govt. Polytechnic Chhapar**

 **Electrical Engineering Department**

 **Lesson Plan**

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| **Name of Faculty** | **Sh. Pardeep Kumar** |
| **Discipline** | **Electrical Engineering** |
| **Semester** | **4th** |
| **Subject** | **Digital Electronics**  |
| **Lesson Plan Duration** | **From March 2022 to June 2022** |
| **Work load [Theory + Practical] Per Week** | **[04+02]** |

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| **Week** | **Day** | **Topic** |
| 1 | 1. | Introduction to subject |
| 2. | Decimal, binary, octal and hexa-decimal number systems |
| 3. | inter-conversion of numbers |
| 4. | Revision |
| 2 | 5. | inter-conversion of numbers |
| 6. | Binary and Hexadecimal addition, subtraction |
| 7. | Binary and Hexadecimal multiplication |
| 8. | Revision |
| 3 | 9. | 1’s and 2’s complement methods of addition/subtraction |
| 10. | 1’s and 2’s complement methods of addition/subtraction |
| 11. | Definition, symbol and truth tables for inverter, OR, AND Gate |
| 12. | Revision |
| 4 | 13. | Definition, symbol and truth tables for NAND, NOR and X-OR Gates |
| 14. | Equivalence circuit (Ex.NOR) |
| 15. | Equivalence circuit (Ex.NOR) |
| 16. | Revision |
| 5 | 17. | Boolean Relations and their applications |
| 18. | DeMorgan’s Theorems |
| 19. | K-Map upto four variables |
| 20. | Revision |
| 6 | 21. | K-Map upto four variables continue |
| 22. | Half adder |
| 23. | Full adder |
| 24. | Revision |
| 7 | 25. | Full adder |
| 26. | Encoder |
| 27. | Decoder |
| 28. | Revision |
| 8 | 29. | Multiplexer / Demultiplexer introduction |
| 30. | Multiplexer |
| 31. | Demultiplexer |
| 32. | Revision |
| 9 | 33. | Display Devices - types |
| 34. | LED |
| 35. | LCD |
| 36. | Revision |
| 10 | 37. | 7-segment display |
| 38. | Flip-Flops Introduction |
| 39. | J-K Flip-Flop |

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|  | 40. | Revision |
| 11 | 41. | R-S Flip-Flop |
| 42. | D-Type Flip-Flop |
| 43. | T-Type Flip-Flop |
| 44. | Revision |
| 12 | 45. | Applications of Flip-Flops |
| 46. | Introduction of Shift Registers and Counters |
| 47. | Registers Continue |
| 48. | Revision |
| 13 | 49. | Counters continue… |
| 50. | A/D converter (Counter ramp, successive approximation method of A/DConversion) |
| 51. | A/D converter (Counter ramp, successive approximation method of A/DConversion) |
| 52. | Revision |
| 14 | 53. | D/A converters (Binary weighted, R-2R D/A Converter) |
| 54. | D/A converters (Binary weighted, R-2R D/A Converter) |
| 55. | Semi-conductor Memories Types, merits, demerits, and applications |
| 56. | Revision |
| 15 | 57. | Revision |
| 58. | Revision |
| 59. | Revision |
| 60. | Revision |

Practical

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| **Week** | **Day** | **Topic** |
| 1. | 1. | Verification and interpretation of truth table for AND, OR, NOT, NAND, NOR,X-OR gates |
| 2. | 2. | Revision |
| 3. | 3. | Construction of Half Adder using gates |
| 4. | 4. | Revision |
| 5. | 5. | Construction of Full Adder using gates |
| 6. | 6. | Revision |
| 7. | 7. | To verify the truth table for JK flip flop |
| 8. | 8. | Revision |
| 9. | 9. | Construction and testing of any counter |
| 10. | 10. | Revision |
| 11. | 11. | Verification of operation of a 8-bit D/A Converter |
| 12. | 12. | Revision |
| 13. | 13. | Revision |
| 14. | 14. | Revision |
| 15. | 15. | Revision |