**Lesson Plan**

**Faculty Name: Pardeep Kumar**

**Discipline: Computer Engg.**

**Semester: 4th**

**Subject: Microprocessor & Peripheral Devices**

**Lesson Plan duration: January 2020 to May 2020 (tentative)**

**Work load (Lecture /Practical) per week (in hours): Lectures—04 Practical-03**

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| **Week** | **Theory** | | **Practical** | |
| **Lecture day** | **Topic Covered**  **(Including Assessment and Sessional)** | **Practical day** | **Topic Covered ( Including Viva-Voce)** |
| 1st | 1. | Introduction to Microprocessor, Evolution of Microprocessor | 1. | Familiarization of different keys of 8085 microprocessor kit and it’s memory map (Gr-A) |
| 2. | Different units of a Microprocessor & Description of each Unit | 2. | Familiarization of different keys of 8085 microprocessor kit and it’s memory map (Gr-B) |
| 3. | Organization of a Microcomputer System, Applications of Microprocessor |
| 2nd | 4. | Introduction to Intel 8085 microprocessor, features, and its Architecture | 3. | Steps to Enter, Modify data/ program and to execute a programme on 8085 kit (Gr-A) |
| 5. | Functional Block Diagram of 8085 and Explanation of each Unit | 4. | Steps to Enter, Modify data/ program and to execute a programme on 8085 kit (Gr-B) |
| 6. | System Buses: Address Bus, Data Bus, Control Bus |
| 3rd | 7. | Pin Diagram of 8085 & Description of each Pin | 5. | Writing and Execution of ALP for addition and Subtraction of two 8-bits numbers (Gr-A) |
| 8. | Demultiplexing of Address/Data Bus, Generation of Read/Write Control signals | 6. | Writing and Execution of ALP for addition and Subtraction of two 8-bits numbers (Gr-B) |
| 9. | Steps to execute a stored programme |
| 4th | 10. | Instruction Cycle, Machine cycle, and T-state, Fetch and Execute Operation | 7. | Writing and Execution of ALP for addition and Subtraction of two 8-bits numbers (Gr-A) |
| 11. | Timing Diagram for Opcode Fetch, Memory Read and Memory Write M/C cycles | 8. | Writing and Execution of ALP for addition and Subtraction of two 8-bits numbers (Gr-B) |
| 12. | Timing Diagram for I/O Read and I/O Write M/C cycles |
| 5th | 13. | **1st Sessional Test** | 9. | **Viva- Voce I (Gr-A)** |
| 14. | Introduction to programming w.r.t 8085, Assembly Language and Machine language | 10. | **Viva- Voce I (Gr-B)** |
| 15. | Instruction, Instruction Formats, Addressing Modes |
| 6th | 16. | Intel 8085 Instructions: Data Transfer group | 11. | Writing and Execution of ALP for Finding the largest or smallest among many 8-bits numbers (Gr-A) |
| 17. | Arithmetic and Logic Group of Instructions | 12. | Writing and Execution of ALP for Finding the largest or smallest among many 8-bits numbers (Gr-B) |
| 18. | Branching & M/C Control group of Instructions |
| 7th | 19. | Programming Techniques: Looping, Counting, and Indexing | 13. | Few Value Added Programming Examples (Gr-A) |
| 20. | Counters & Time Delays | 14. | Few Value Added Programming Examples (Gr-B) |
| 21. | Stack & Subroutine |
| 8th | 22. | Introduction to Interfacing: Logic Devices for Interfacing | 15. | Writing and Execution of ALP for arranging 10 numbers in ascending/ descending order (Gr-A) |
| 23. | Memory Interfacing: Address Decoding and Interfacing Circuit | 16. | Writing and Execution of ALP for arranging 10 numbers in ascending/ descending order (Gr-B) |
| 24. | Memory map of 8085 Microprocessor, Memory mapped I/O, and I/O Mapped I/O Schemes |
| 9th | 25. | I/O Interfacing, Interfacing I/O Devices using Decoders | 17. | **Viva-Voce II (Gr-A)** |
| 26. | **2nd Sessional Test** | 18. | **Viva-Voce II (Gr-B)** |
| 27. | Interrupts: Definition, Sequence of Interrupt Operation, Interrupt Classification |
| 10th | 28. | 8085 H/W Interrupts: TRAP, RST 7.5, RST 6.5, RST 5.5, INTR | 19. | Writing and Execution of ALP for 0 TO 9 BCD Counters (Gr-A) |
| 29. | S/W Interrupts, Instructions for handling Interrupts: RIM, SIM,EI, DI | 20. | Writing and Execution of ALP for 0 TO 9 BCD Counters (Gr-B) |
| 30. | Data Transfer Techniques: Programmed, DMA, Synchronous and Asynchronous Data Transfer schemes |
| 11th | 31. | Interrupt driven data Transfer scheme | 21. | Interfacing Exercise on 8255 like LED Display Controller (Gr-A) |
| 32. | Direct Memory Access(DMA) Scheme of data transfer and it’s types | 22. | Interfacing Exercise on 8255 like LED Display Controller (Gr-B) |
| 33. | Programmable Peripheral Devices: 8255 PPI |
| 12th | 34. | 8253 PIT | 23. | Interfacing Exercise on 8253 Programmable Interval Timer (Gr-A) |
| 35. | 8257/8237 DMA Controller | 24. | Interfacing Exercise on 8253 Programmable Interval Timer (Gr-B) |
| 36. | 8279 Programmable Keyboard display Interface |
| 13th | 37. | 8251 Communication Interface Adapter | 25. | **Viva Voce III(GR-A)** |
| 38. | **3rd Sessional Test** | 26. | **Viva Voce III(GR-B)** |
| 39. | **Revision** |